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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
P2002,0892	10/689,419

Applicant: Martin Perner

Filing Date	Group Art Unit
October 20, 2003	~~2812~~ 2829

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

VN	O	Dae-Young Jung et al. :Reusable Embedded Debugger for 32bit RISC Processor Using the JTAG Boundary Scan Architecture", Proceedings of the 2002 IEEE Asia Pacific Conference on ASIC, 2002, pp. 209-212
VN	P	E. de la Torre et al.: "Non-intrusive debugging using the JTAG interface of FPGA-based prototypes", Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, 2002, pp. 666-671

EXAMINER	DATE CONSIDERED
Nguye	04/28/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.